What is claimed is:

1. A charge pump circuit comprising:

a first switching element having a gate, a drain, and a source connected to ground, and being activated when a down signal is inputted to said gate;

a second switching element having a gate, a drain, and a source connected to power source, and being activated when an up signal is inputted to said gate;

a discharging element having a gate, a drain, and a source connected to said drain of the first switching element, and controlling a quantity of current outputted to said drain according to a biasing voltage applied to said gate;

a charging element having a gate, a drain, and a source connected to said drain of the second switching element, and controlling a quantity of current outputted to said drain according to a bias voltage applied to said gate;

a biasing unit having the first and second terminals connected to said gate of said discharging and charging elements, and outputting a bias voltage which activate said discharging and charging elements to said first and second terminals, respectively;

a first compensating unit having an input terminal, a control terminal, and an output terminal connected to said gate of discharging element, and discharging to said output terminal when said down signal is applied to said input terminal, and controlling a quantity discharged to said output terminal by a first control signal applied to said control terminal; and

a second compensating unit having an input terminal, a control terminal, and an output terminal connected to said gate of charging element, and charging to said output terminal when said up signal is applied to said input terminal, and controlling a uantity charged to said output terminal by a second control signal applied to said control terminal.

2. The charge pump circuit of claim 1, wherein said first and second compensating units comprise a buffer and a capacitor, respectively, and wherein input terminals of said buffer form said input terminals of said first and second compensating units, respectively, and output terminals are connected to one terminal of said capacitors, respectively, and the other terminal of said capacitors form said output terminal of said first and second compensating units, respectively, and a high level control terminal of said buffer of said first compensating unit and a low level control terminal of said buffer of said second compensating unit form said control terminals of said first and second compensatings, respectively.

3. A charge pump circuit comprising:

a first switching element having a gate, a drain, and a source connected to ground, and being activated when a down signal is inputted to said gate;

a second switching element having a gate, a drain, and a source connected to power source, and being activated when an up signal is inputted to said gate;

a discharging element having a gate, a drain, and a source connected to

said drain of the first switching element, and controlling a quantity of current outputted to said drain according to a biasing voltage applied to said gate;

a charging element having a gate, a drain, and a source connected to said drain of the second switching element, and controlling a quantity of current outputted to said drain according to a bias voltage applied to said gate;

a biasing unit having the first and second terminals connected to said gate of discharging and charging elements, and outputting a bias voltage which activate said discharging and charging elements to said first and second terminals, respectively;

a first compensating unit having an input terminal, and an output terminal connected to said source of discharging element, and charging to said output terminal when said down signal is applied to said input terminal; and

a second compensating unit having an input terminal, and an output terminal connected to said source of charging element, and discharging to said output terminal when said up signal is applied to said input terminal.

4. The charge pump circuit of claim 3, wherein said first and second compensating units comprise a invertor and a capacitor, respectively, and wherein

input terminals of said invertors form said input terminals of said first and second compensating units, respectively, and output terminals are connected to one terminal of said capacitors, respectively, and the other terminal of said capacitors form said output terminal of said first and second compensating units,

respectively.

5. A charge pump circuit comprising:

a first switching element having a gate, a drain, and a source connected to ground, and being activated when a down signal is inputted to said gate;

a second switching element having a gate, a drain, and a source connected to power source, and being activated when an up signal is inputted to said gate;

a discharging element having a gate, a drain, and a source connected to said drain of the first switching element, and controlling a quantity of current outputted to said drain according to a biasing voltage applied to said gate;

a charging element having a gate, a drain, and a source connected to said drain of the second switching element, and controlling a quantity of current outputted to said drain according to a bias voltage applied to said gate;

a biasing unit having the first and second terminals connected to said gate of discharging and charging elements, and outputting a bias voltage which activate said discharging and charging elements to said first and second terminals, respectively;

a first compensating unit having an input terminal, a control terminal, and an output terminal connected to said gate of discharging element, and discharging to said output terminal when said down signal is applied to said input terminal, and controlling a quantity discharged to said output terminal by a first control signal applied to said control terminal;

a second compensating unit having an input terminal, a control terminal, and an output terminal connected to said gate of charging element, and charging to said output terminal when said up signal is applied to said input terminal, and controlling a quantity charged to said output terminal by a second control signal applied to said control terminal;

a first switch means connected to between said first terminal of said biasing unit and said gate of said discharging element, and a second switch means connected to between said second terminal of said biasing unit and said gate of said charging element;

a first control unit being connected to between said first terminal of said biasing unit and said gate of said discharging element, and generating said first control signal so that voltage of said first terminal of said biasing unit is substantially identical to voltage of said gate of said discharging element when said first switch means is opened; and

a second control unit being connected to between said second terminal of said biasing unit and said gate of said charging element, and generating said second control signal so that voltage of said second terminal of said biasing unit is substantially identical to voltage of said gate of said charging element when said second switch means is opened.

6. The charge pump circuit of claim 5, wherein said first and second compensating units comprise a buffer and a capacitor, respectively, and wherein input terminals of said buffers form said input terminals of said first and second

compensating units, respectively, and output terminals are connected to one terminal of said capacitors, respectively, and the other terminal of said capacitors form said output terminal of said first and second compensating units, respectively, and a high level control terminal of said buffer of said first compensating unit and a low level control terminal of said buffer of said second compensating unit form said control terminals of said first and second compensating units, respectively.

7. The charge pump circuit of claim 5, wherein said first control unit comprises a comparator, a switch means, and an integrator, and wherein

+ input terminal of said comparator is connected to said first terminal of said biasing unit, and

input terminal of said comparator is connected to said gate of said discharging element, and said switch means is connected to between an output terminal of said comparator and an input terminal of said integrator, and said first control signal is outputted to an output terminal of said integrator.

8. The charge pump circuit of claim 5, wherein said second control unit comprises a comparator, a switch means, and an integrator, and wherein

+ input terminal of said comparator is connected to said gate of said charging element, and

input terminal of said comparator is connected to said second terminal of said biasing unit, and said switch means is connected to between an output terminal of said comparator and an input terminal of said integrator, and said

second control signal is outputted to an output terminal of said integrator.

9. A charge pump circuit comprising:

a charge pumping unit having a first and second input terminals, bias terminals, and output terminals, and charging and discharging to a capacitor connected to said output terminals, and setting up the current flowing to said ouput terminals in response to bias voltage applied to said bias terminals;

a current mirror unit having a bias terminal and an output terminal, and taking a current flowing to said output terminal of a charge pumping unit, and controlling a voltage of said output terminal in response to bias voltage applied to said bias terminals;

a contol unit having a first input terminal connected to said output terminal of said charge pumping unit, a second input terminal connected to said output terminal of said circuit mirror unit, and an out terminal, and cotrolling a control current flowing to said output terminal in response to a difference of voltage between said first and said second input terminals; and

a biasing unit having a control terminal connected to said output terminal of said control unit, an output terminal connected to said bias terminals of said charge pumping unit, and said current mirror unit, and controlling a voltage of said output terminal in response to said control current flowing to said control terminal.

10. The charge pump circuit of claim 9, wherein said charge pumping unit comprises a first and second PMOS transistors and a first and second NMOS

transistors, and wherein

gates of said first PMOS and NMOS transistors form said first and second input terminals of said charge pumping unit, respectively, and drains of said first PMOS and NMOS transistors are connected to sources of said second PMOS and NMOS transistors, respectively, and sources of said first PMOS and NMOS transistors are connected to power source and ground, respectively; and

a gate of said second PMOS transistor forms said bias terminal of said charge pumping unit and is connected to a drain of said second NMOS transistor and forms said output terminal of said charge pumping unit, and a constant N type bias voltage is applied to a gate of said second NMOS transistor.

11. The charge pump circuit of claim 9, wherein said current mirror unit comprises a first and second PMOS transistors and a first and second NMOS transistors, and wherein

gates of said first PMOS and NMOS transistors are connected to ground and power source, respectively, and drains of said first PMOS and NMOS transistors are connected to sources of said second PMOS and NMOS transistor, respectively, and sources of said first PMOS and NMOS transistors are connected to power source and ground, respectively; and

said gate of said second PMOS transistor forms said bias terminal of said current mirror unit, and said drain of said second PMOS transistor is connected to said drain of said second NMOS transistor and forms said output terminal of said current mirror unit, and said N type bias voltage is applied to said gate of

said second NMOS transistor.

12. The charge pump circuit of claim 9, wherein said contol unit has ±input terminals which form said first and second input terminals of said control unit, and output terminal, and comprises a comparator which controls a voltage of said output terminal by a difference of the voltage applied to said ±input terminals and PMOS transistor; and

a source of said PMOS transistor is connected to power source, and a gate of said PMOS transistor is connected to said output terminal of said comparator, and a drain of said PMOS transistor forms said output terminal of said control unit.

13. The charge pump circuit of claim 9, wherein said biasing unit comprises a first and second PMOS transistors and a first and second NMOS transistors, and gates of said first PMOS and NMOS transistors are connected to ground and power source, respectively, and drains of said first PMOS and NMOS transistors are connected to sources of said second PMOS and NMOS transistor, respectively, and sources of said first PMOS and NMOS transistors are connected to power source and ground, respectively; and

said gate of said second PMOS transistor forms said output terminal of said biasing unit, and said drain of said second PMOS transistor is connected to said drain of said second NMOS transistor and forms said control terminal of said biasing unit, and said gate and drain of said second PMOS transistor are connected to each other, and said N type bias voltage is applied to said gate of

said second NMOS transistor.

14. The charge pump circuit of claim 9, wherein said charge pumping unit comprises a first and second PMOS transistors and a first and second NMOS transistors, and gates of said first PMOS and NMOS transistors form said first and second input terminals of said charge pumping unit, respectively, and drains of said first PMOS and NMOS transistors are connected to power source and ground, respectively; and

a gate of said second NMOS transistor forms said bias terminal of said charge pumping unit, and a drain of said second NMOS transistor is connected to said drain of said second PMOS transistor and forms said output terminal of said charge pumping unit, and a constant P type bias voltage is applied to said gate of said second PMOS transistor.

15. The charge pump circuit of claim 9, wherein said current mirror unit comprises a first and second PMOS transistors and a first and second NMOS transistors, and gates of said first PMOS and NMOS transistors are connected to ground and power source, respectively, and drains of said first PMOS and NMOS transistors are connected to sources of said second PMOS and NMOS transistor, respectively, and sources of said first PMOS and NMOS transistors are connected to power source and ground, respectively; and

said gate of said second NMOS transistor forms said bias terminal of said current mirror unit, and said drain of said second NMOS transistor is connected to said drain of said second PMOS transistor and forms said output terminal of

said current mirror unit, and said P type bias voltage is applied to said gate of said second PMOS transistor.

16. The charge pump circuit of claim 9, wherein said contol unit has ±input terminals which form said first and second input terminals of said control unit, and output terminal, and comprises a comparator which controls voltage of said output terminal by a difference of the voltage applied to said ±input terminals and NMOS transistor; and

a source of said NMOS transistor is grounded, and a gate of said NMOS transistor is connected to said output terminal of said comparator, and a drain of said NMOS transistor forms said output terminal of said control unit.

17. The charge pump circuit of claim 9, wherein said biasing unit comprises a first and second PMOS transistors and a first and second NMOS transistors, and gates of said first PMOS and NMOS transistors are connected to ground and power source, respectively, and drains of said first PMOS and NMOS transistors are connected to sources of said second PMOS and NMOS transistor, respectively, and sources of said first PMOS and NMOS transistors are connected to power source and ground, respectively; and

said gate of said second NMOS transistor forms said output terminal of said biasing unit, and said drain of said second NMOS transistor is connected to said drain of said second PMOS transistor and forms said control terminal of said biasing unit, and said gate and drain of said second NMOS transistor are connected to each other, and said P type bias voltage is applied to said gate of

said second PMOS transistor.